REMARKS:

This paper is herewith filed in response to the Examiner's Office Action mailed on July 24, 2007 for the above-captioned U.S. Patent Application. This office action is a rejection of claims 1-34 of the application.

More specifically, the Examiner has objected to claims 2-10, 12-20, 22-31, 33, and 34 because of informalities; has rejected claims 1-4, 8-14, 18-24, and 28-34 under 35 USC 102(b) as anticipated by Svensson (IEEE Journal of solid-state circuits: A 3-level Asynchronous Protocol for a differential Two-Wire communication link); and rejected claims 5-7, 15-17, and 25-27 under 35 USC 103(a) as being unpatentable over Svensson in view of Huang (US5,798,535). The Applicants respectfully traverse the rejection.

In regards to the objections to claims 2-10, 12-20, 22-31, 33, and 34, these claims have been amended as suggested by the Examiner. The objections are seen as overcome and the objections should be removed.

Regarding the rejections under 35 USC 102(b) the Applicants respectfully disagree with the Examiner.

The Applicants respectfully note that claims 1, 3, 11, 13, 21, 23, 32, and 34 have been amended for mere clarification. Support for the amendments can be found at least on page 6, lines 10-24 and page 7, lines 3-13. No new matter is added.

In the rejection of claim 1 the Examiner states:

> "Re claim 1, Svensson discloses **a Multi-level Analog Signaling method** comprising encoding data bits represented by multi-level analog signals (page 1130; section A, "encoder and driver"); **transmitting the encoded data bits over at least two multi-level signal buses between a transmitter and a receiver such that (fig.1, two-wire link), on each multi-level signal bus**, during each data bit period the signal level is required to change from a first signal level to a

> second, different signal level (fig. 1 page 1129, section II, "a balanced two-wire link carrying a three-state code"); **and indicating a data boundary to the receiver by holding one of the multi-level signal buses at the same level for at least two consecutive bit periods (page 1130, section B, clock extractor"),"** (emphasis added).

The Applicants note that Svensson is discussed on page 2 of the specification.

Further, the Applicants note that claim 1 has been amended for clarification to recite in part:

> "A Multi-level Analog Signaling (MAS) method comprising encoding data bits represented by multi-level analog signals comprising more than two analog amplitude levels."

As cited Svensson discloses:

> "**The most straight and efficient design of the encoder** is to use a bi-directional register ring which consists of three registers. In the ring, a pattern of "0-0-1" is stored and clocked back and forth, controlled by the data. **Two outputs** are taken from the same ring at different registers **to form states (O_1, O_2)**, i.e., (0, 1), (1, 0) and (0, 0)," (emphasis added), (page 1130, section A).

The Applicants respectfully note that Svensson merely discloses that outputs O_1 and O_2 are each capable of the two levels 0 and 1. The Applicants contend that Svensson does not disclose multi-level analog signals comprising more than two amplitude levels as in claim 1. The Applicants note that this distinction is clearly illustrated in Fig. 1 where Svensson clearly shows **only two levels of 0 and 1 on O_1 and O_2**.

Further, the Applicants contend that in Svensson just because the outputs O_1 and O_2 can be encoded with **three possible variations** of levels "i.e., (0, 1), (1, 0) and (0, 0)," Svensson still can not be seen to disclose **encoding** data bits represented by multi-level analog signals comprising **more than two analog amplitude levels** as in claim 1.

The Applicant contends that for at least these reasons Svensson can not be seen to

disclose "**encoding** data bits represented by multi-level analog signals **comprising more than two analog amplitude levels**," as in claim 1.

Additionally, in regards to the rejection of claim 1 where it is stated that Svensson discloses "**indicating a data boundary to the receiver by holding one of the multi-level signal buses at the same level for at least two consecutive bit periods (page 1130, section B, clock extractor")**," the Applicants disagree with the Examiner.

As cited Svensson discloses:

> "The clock can be recovered by an asyncronous finite state machine without the need of any oscillator. The synthesis of the finite state machine can be done **by using systematic methods**, for example, introduced in [9]. If we look at **the codes received**, the clock can be extracted from their OR results (or NOR results), **as long as half of them are reversed by a control signal, as shown in Fig. 6**. The task is to detect the borders where the OR results should be reversed **and to create the control signal**. An edge-triggered flip-flop connected in a divide-by-two circuit mode can be used to produce the control signal," (page 1130, section B).

The Applicants note that here Svensson appears to be **generating at the receiver** a control signal that is used for the clock recovery of **a received signal (O_1, O_2)**.

For at least the reasons stated the Applicants contend that Svensson can not be seen to disclose **indicating to a receiver a data boundary** by holding one of the multi-level signal buses at the same level for at least two consecutive bit periods as in claim 1.

Further, the Applicants respectfully note that a 35 USC 102(b) rejection requires that the cited art **disclose to the specificity of the rejected claim**; Verve, LLC v. Crane Cams, Inc., 311 F.3d 1116, 1120, 65 USPQ2d 1051 (Fed. Cir. 2002) ("**A single reference must describe the claimed invention with sufficient precision and detail to establish that the subject matter existed in the prior art**"). Therefore, it is axiomatic that a 35 USC 102(b) rejection requires strict identity with every claim element.

The Applicants contend that for at least the reasons stated Svensson clearly can not be seen to disclose "**encoding data bits** represented by multi-level analog signals **comprising more than two analog amplitude levels**; transmitting the encoded data bits **over at least two multi-level signal buses** between a transmitter and a receiver such that, on each multi-level signal bus, during each data bit period the signal level is required to change from a first signal level to a second, different signal level; and **indicating a data boundary to the receiver** by holding one of the multi-level signal buses at the same level for at least two consecutive bit periods," as in claim 1. Thus, the rejection of claim1should be removed and claim 1 should be allowed.

In addition, for at least the reasons already stated Svensson can not be seen to disclose at least where independent claim 11 recites in part "a transmitter to **encode data bits** represented by multi-level analog signals **comprising more than two analog amplitude levels**; **at least two multi-level signal buses** coupled between said transmitter and a receiver for conveying the encoded data bits such that, on each multi-level signal bus, during each data bit period the signal level is required to change from a first signal level to a second, different signal level; **said transmitter indicating a data boundary** to said receiver **by holding one of the multi-level signal buses** at the same level for at least two consecutive bit periods."

Furthermore, for at least the reasons already stated Svensson can not be seen to anticipate at least where independent claim 21 recites in part "a transmitter **to encode data bits** represented by multi-level analog signals **comprising more than two analog amplitude levels**; where a data communications bus that couples the transmitter to a receiver in another port comprises**at least two multi-level signal buses** for conveying the encoded data bits such that, on each multi-level signal bus, during each data bit period the signal level is required to change from a first signal level to a second, different signal level; **said transmitter indicating a data boundary** to said receiver by **holding one of the multi-level signal buses of the at least two multi-level signal buses** at the same level for at least two consecutive bit periods."

Further, for at least the reasons already stated Svensson can not be seen to anticipate at least

where independent claim 32 recites in part "**encoding data bits** represented by multi-level analog signals **comprising more than two analog amplitude levels**; **at least two multi-level signal bus means** coupled between said transmitter means and receiver means for conveying the encoded data bits such that, on each multi-level signal bus means, during each data bit period the signal level is required to change from a first signal level to a second, different signal level; **said transmitter means indicating a data boundary** to said receiver means **by holding one of the multi-level signal buses** at the same level for at least two consecutive bit periods."

Regarding the rejection of claim 2 under 35 USC 102(b) the Examiner states:

> "Re claim 2, the method as in claim 1, where encoding includes, when a data bit to be encoded is the same as the data bit encoded for an immediately prior bit period, **encoding instead a strobe signal** represented by a predetermined one of the levels of the multi-level analog signal (fig.6, page 1130 section A, "encoder and driver"), **where the presence of the strobe signal** at the receiver is used to generate a clock edge (page 1130, section B, "clock extractor")."

Firstly, the Applicants note that as stated above the "clock extractor," as cited by the Examiner in the rejection of claim 2, **is located at the receiver** and is used for the clock **recovery** of **a received signal** (O_1, O_2). The Applicants contend that as cited Svensson can not be seen to be "**encoding instead** a strobe signal," as in claim 2.

Therefore, for at least the reasons stated the Applicants contend that Svensson does not disclose claim 2 and the rejection of claim 2 should be removed.

In addition, for at least the reasons stated the reference can not be seen to anticipate at least where claim 3 recites in part "where two analog signal levels convey the encoded data bits **and a third analog signal level conveys the strobe signal**."

Further, for at least the reasons stated the reference can not be seen to anticipate at least where claim 12 recites in part "when a data bit to be encoded is the same as the data bit encoded for an immediately prior bit period, **the transmitter instead encodes a strobe signal** represented by a predetermined one of the levels of the multi-level analog signal, where **the presence of the**

strobe signal at said receiver is used to generate a clock edge."

In addition, for at least the reasons stated the reference can not be seen to anticipate at least where claim 13 recites in part "where two analog signal levels convey the encoded data bits and **a third analog signal level conveys the strobe signal**."

In addition, for at least the reasons stated the reference can not be seen to anticipate where claim 22 recites in part "when a data bit to be encoded is the same as the data bit encoded for an immediately prior bit period, **the transmitter instead encodes a strobe signal** represented by a predetermined one of the levels of the multi-level analog signal, **where the presence of the strobe signal** at said receiver is used to generate a clock edge."

Further, for at least the reasons stated the reference can not be seen to anticipate at least where claim 23 recites in part "where two analog signal levels convey the encoded data bits and **a third analog signal level conveys the strobe signal**."

Furthermore, for at least the reasons stated the reference can not be seen to anticipate where claim 33 recites in part "when a data bit to be encoded is the same as the data bit encoded for an immediately prior bit period, said **encoding means instead encodes a strobe signal** represented by a predetermined one of the levels of the multi-level analog signal, **where the presence of the strobe signal** at said receiver means is used to generate a clock edge."

In addition, for at least the reasons stated the reference can not be seen to anticipate at least where claim 34 recites in part "where two analog signal levels convey the encoded data bits and **a third analog signal level conveys the strobe signal**."

In addition, for at least the reason that claims 3-4 and 8-9; claims 12-14 and 18-20; claims 22-24 and 28-31; and claims 33-34 depend from claims 1, 11, 21, and 32, respectively, the Applicants contend that Svensson can not be seen to anticipate all the claims 1-4, 8-14, 18-24, and 28-34. The Applicants contend that for at least the reasons stated the rejection of all claims 1-4, 8-14,

18-24, and 28-34 under 35 USC 102(b) should be removed.

Regarding the rejection of claims 5-7, 15-17, and 25-27 under 35 USC 103(a) as being unpatentable over Svensson in view of Huang the Applicants disagree with the rejections.

The Applicants note that Huang relates to "arrays of light emitting devices and more particularly to a novel drive circuitry for the array," (col. 1, lines 6-8). However, although the Applicants do not acquiesce that the combination of Svensson and Huang is feasible, the Applicants contend that Huang at least fails to address a shortfall of Svensson as stated above.

The Applicants contend that for at least the reasons stated even if Svensson were combined with Huang the result would still not disclose or suggest the claims. Thus, the rejections of 5-7, 15-17, and 25-27 under 35 USC 103(a) are seen as improper and the rejections of the claims should be removed.

Based on the above explanations and arguments, it is clear that the references cited cannot be seen to disclose or suggest claims 1-34. The Examiner is respectfully requested to reconsider and remove the rejections of claims 1-34 and to allow all of the pending claims 1-34 as now presented for examination.

For all of the foregoing reasons, it is respectfully submitted that all of the claims now present in the application are clearly novel and patentable over the prior art of record. Should any unresolved issue remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted:

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10/10/2007

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